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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,506	06/09/2005	Keiichi Murakami	2005-0874A	7098

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EXAMINER	
PHAN, THIEM D	
ART UNIT	PAPER NUMBER
3729	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,506	MURAKAMI, KEIICHI	
	Examiner	Art Unit	
	THIEM PHAN	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/11/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 05/01/09 has been fully considered and made of record.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-8 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keiichi Murakami (JP 2000-332387), hereinafter '387.

Regarding claim 1, the '387 teaches a method of producing multilayer printed circuit board, comprising the steps of:

- obtaining a printed wiring board (Fig. 3, 10) with a circuit pattern (Fig. 4, 15) formed on a surface of the printed wiring board;
- forming a resin layer (Fig. 6, 16; Paragr. 17) by superposing a semi-cured resin sheet on the surface of the printed wiring board containing said circuit patterns;
- pressing and forcing the resin layer into spaces between said circuit patterns (Fig. 7, 15);
- curing said resin layer (Paragr. 18); and
- polishing said cured resin layer, thereby exposing said circuit patterns (Paragr. 19);

except for having the complementary resin circuit patterns complementary to said circuit patterns formed on the semi-cured resin sheet, facing and superposing said circuit patterns.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to have the complementary resin circuit patterns complementary to said circuit patterns formed on the semi-cured resin sheet, facing and superposing said circuit patterns because applicant has not disclose that having the complementary resin circuit patterns complementary to said circuit patterns formed on the semi-cured resin sheet, facing and superposing said circuit patterns provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with a resin layer (Fig. 6, 16) on the printed wiring board because it fills spaces between circuit patterns (Fig. 6, 15) as well.

Therefore, it would have been an obvious matter of design choice without obvious benefits to modify the '387 to obtain the invention as specified in Claim 1 as well.

Regarding claim 3, the '387 teaches that the pressing against said resin layer is performed in a reduced pressure atmosphere (Paragr. 17).

Regarding claim 4, the '387 teaches that a metallic foil (Fig. 6, 17) with a roughened surface facing said resin layer is superposed and pressed on said resin layer.

Regarding claim 5, the '387 teaches that the metallic foil (Fig. 6, 17) is formed with a metal of a different kind than said circuit patterns (15).

Regarding claim 6, the '387 teaches that the metallic foil is formed from a nickel material (Fig. 6, 17, Paragr. 17).

Regarding claims 7 and 8, the '387 teaches that the semi-cured resin sheets (Fig. 6, 16; Paragr. 16) are formed from a thermosetting epoxy resin.

Regarding claim 20, the '387 teaches that circuit patterns are formed by an etching method (Paragr. 15).

Response to Arguments

4. Applicant's arguments filed on 5/01/09 have been fully considered but they are not persuasive for the following reasons:

Applicants' assertions (Remarks, pages 5-8) that it is not design choice to have the resin patterned inversely to the circuit because the specification discloses a reason for the resin pattern are traversed. The prior art Murakami teaches the depositing of resin layer (Fig. 6. 16) far above the circuit pattern (15) and the heat and pressure from the plate (17) in low atmospheric pressure will definitively press the resin in every area of the circuit pattern, regardless of dense or nondense areas of circuit pattern because only the plate pressure (17) against the thick layer of resin (16) in a vacuum environment can force the resin into dense mode. By having the resin shaped inversely to the circuit or the resin layered flat high above the circuit or shaped seesaw above the circuit or the resin layered in any shape above the circuit as desired choice, the heat and pressure from the plate (17) in low atmospheric pressure still provide the same result by pressing the resin in every area of the circuit pattern, regardless of dense or nondense areas of circuit pattern. Therefore, having a resin shaped inversely to the circuit is not productive because it creates more costs without any advantage over pressing the deposited resin above the circuit pattern, as taught by Murakami.

According to MPEP 716.02(f), there is a requirement that there must be an advantage disclosed or inherent in order to proper define the logic or reasoning such as the application of

resin layer being shaped inversely to the circuit for critical application or value. From the paragraph above, it appears that there is no advantage disclosed in forming the resin layer being shaped inversely to the circuit and there is no inherency of critical application of them either. Therefore, there is no advantage as defined under MPEP 716.02(f).

Claims 3-8 and 20 stand rejected as provided in section 3 and with respect to the responses above.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M & Tu, 6AM - 2PM, and W & Th, 9AM – 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derris Banks can be reached on 571-272-4419. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Phan Thiem/
Primary Examiner, Art Unit 3729

July 7, 2009